

Implementation of Digital Pulse Width Modulators Using Frequency Divider Method in FPGA

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Abstract - The Digital pulse width modulators are used for digital control applications. When the requirement of clock frequency exceeds the required limit the switching frequency of the power converter also increased. In this paper a new architecture for digital pulse width modulator is proposed. The proposed method is based on digital clock manager which is present in the Spartan 3 FPGA. The architecture will be implemented in FPGA Spartan 3 and the performances are verified.

Keywords: DPWM- Digital Pulse Width Modulator, FPGA- Field Programmable Gate Array, DCM- Digital Clock Manager, and Phase shift

I. INTRODUCTION

Pulse width modulation is the modulation technique which changes the width of the pulse based on the modulator signal. Now a days this technology is used for control applications. The main use is to control the power supply to the electrical devices. The digital pulse width modulators are the basic building block in digital control applications. The advantages of DPWM are reliability, flexibility and expandability and it is independent of aging.

Several DPWM architectures are proposed, which are counter based plus digital clock manager (DCM) block which is present in Spartan 3 FPGAs. The main applications of PWM are DC-DC converters. In recent developments in semiconductor technology we use higher switching frequencies through Sic and GaN. This technology will reduce the size and cost of power converters.

PWM uses as a voltage regulator, the duty cycle and switching delays can be tuned accurately. The DC-DC converters are used to control the battery powered devices such as mobile phones, digital cameras, and speed control applications. This converters has low switching frequency compared with analog controllers. [2] In this method both synchronous and asynchronous blocks are used. Synchronous block is based on counter.

In some applications SMPS circuits are used to supply power to the circuits and it has the following advantages such as programmability, component count is reduced, and it is independent of aging. The two disadvantages of digital control are sampling or processing delay and limited resolution. To overcome this disadvantages the different solutions have been proposed and is implemented in digital signal processor (DSP). And in application specific integrated circuits, or field programmable gate array (FPGA). This method is based on counters to increase the linearity [31]. In order to obtain resolution delay lines are used.

In DSPs, HRPWM peripherals are included and it extends the capacity of time resolution. Several architectures are proposed for IC implementation they are all based in tap delay line with multiplexer or delay line or a hybrid counter

In this literature several FPGA-based solutions are proposed. One common technique is coarse resolution counter stage and digital clock manager block architecture. Beginning of the counter period the PWM signal is set, and the signal is reset after the clock cycles reaches the

maximum value. In previous methods the generation of reset signal is not synchronous. In asynchronous method it is hard to calculate timing, routing and timing analysis during implementation. The synchronous design the reliability of the circuit is increased, and the design process is not difficult. The proposed system is referred from the reference[1] and then modification using CADENCE is given below.

The aim of this paper is to design a new architecture for digital pulse width modulator based on counter and comparator and DCM blocks present in FPGA.

II. METHODOLOGY

A. DCM Architecture

DCM blocks are present in Spartan 3 FPGA series kits. DCM blocks maintains the clocking functions in FPGAs. Internal architecture of the DCM has Phase shifter, Delay taps, and DLL.

The DCM has the following features:

1. Phase Shifting: The DCM provides four phase shifting clock outputs of different phases with respect to input clock signal. The DCM blocks provide CLK0, Clk90, clk180, and clk270. Clk360 is same as clk0.
2. Frequency Synthesizer: The DCM provides a more number of outputs by multiplying and dividing the clock signal.

Two types of phase shifting are there Fine Phase shifting can be fixed or variable. In fixed phase shifting the phase shifting value range varies between (-255 to +255). In variable phase shifting several clock cycles is needed for changing the duty cycle. Variable phase shifting is done in asynchronous circuit. In this paper fully synchronous circuit with fixed phase shifting is proposed. The source clock is given as an input and the four phase shifted clocks are the output of DCM blocks. One of the clock output from DCM is given as counter input. The counter counts number of clock cycles from DCM output, the clock value reaches maximum value the counter will be reset and it starts from 0.

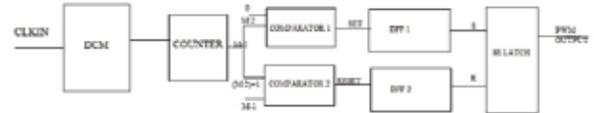


Fig.1 DCM based PWM.

The duty cycle command has ranging from 0 to m, the counter has m-1 bits. The SET signal is set when counter value is ranging from 0 to M/2. The SR latch is set when comparator1 is active. When the counter value ranges from (M/2) +1 to M-1 SR latch is reset when the comparator2 is active. The counter value reaches maximum the counter will be reset.

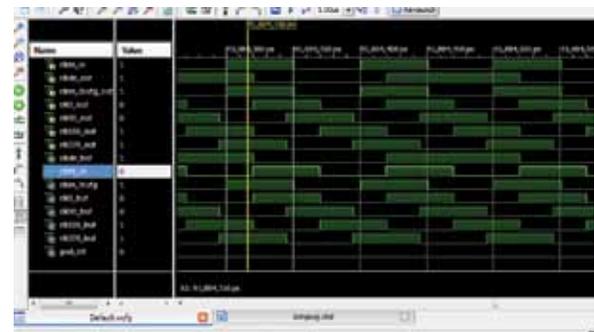


Fig.2 DCM Phase shifted output

Above waveform shows the DCM output waveform. The counter value is equal to M-1, CLR signal is activated. For a single clock pulse input, it produces four phase shifted outputs. Each clock signal output is phase shifted with regular interval. The interval is based on fixed or variable phase shift mode. The advantage of this method is to generate the reset signal for SR latch is synchronous. One of the four phase shifted clock output is fed to the counter as an input.

III. PROPOSED SYSTEM

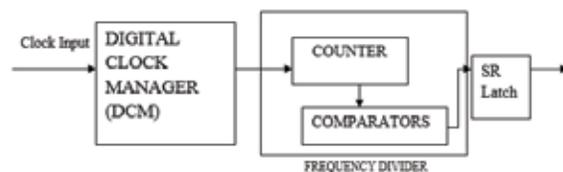


Fig.3 PWM Using Frequency Divider Circuit

In this proposed system a new architecture is designed for Pulse Width Modulator using Digital Clock Manager (DCM) block which is already present in FPGA. Phase shifter, frequency synthesizer, delay lines are the basic operations performed by DCM block. One of the DCM clock output is given as an input for Clock DIV circuit. Which divides the clock time period based on N value. The DCM circuit is connected with CLKDIV circuit. DCM block produces phase shifted clock outputs.

The advantage of this proposal in relation to others is that the digital circuit that generates the reset of the SR latch is synchronous. The use of asynchronous circuits to reset the latch makes harder to calculate timing using static timing analysis and can result in glitching since controlling the logic and routing delays in an FPGA is more difficult than in ASIC implementations.

The CLR signal is set when the counter is equal to the N MSBs of dc. The SET signal is set when the counter is zero and dc is different from zero. These signals are used to generate the SET and RESET signals that control the SR latch.

CLK0 output is same as CLKIN and other outputs are phase shifted with respect to its delay value. Four different phase shifted clock outputs are produced by DCM blocks. When the clock pulse reaches its maximum value the counter value is set to 0. The SET signal is activated. And the counter value reaches the maximum counter will be RESET and the CLR signal is activated.

One of the DCM output clock is given as an input to clock divider circuit. Clock divider is a circuit which performs the counter and comparator operations. Output of clock divider circuit is given to the input of SR latch.

A clock divider is otherwise called as frequency divider, also called scaler, is a circuit that takes an input signal of a frequency f , and generates an output signal frequency

$$f_{out} = \frac{f_{in}}{n} \quad (1)$$

Where n an integer, Phase-locked loop frequency synthesizers is make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog

and digital applications. Analog frequency dividers are less common and used only at very high frequencies. Digital dividers implemented in modern IC technologies can work up to tens of GHz.

Counter is a device which counts the number of times a particular event or process has occurred, often in relationship to a clock signal. In this Synchronous counter is used. All state bits change under control of a single clock. In this 8-bit counter is used and the pulse width modulation output is taken from the counter. In a synchronous counter, the input pulses are applied to all clock pulse inputs of all flip flops simultaneously (directly). Synchronous counter is also known as parallel sequential circuit. In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). Synchronous counters can be implemented with hardware finite state machines, which are more complex but allow for smoother, more stable transitions.

IV. SIMULATION AND RESULTS

In this section, the simulation result obtain form proposed (hybrid difference) method is discussed. Software tool used to code this method is Xilinx 14.5 using vhdl program and simulated in Isim simulator.

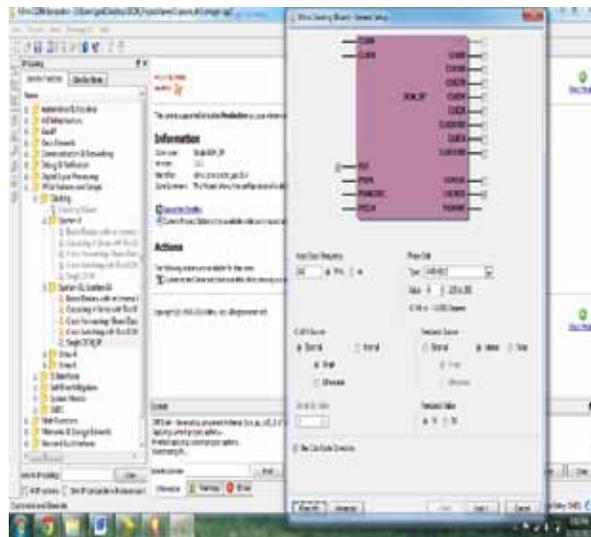


Fig.4 Generation of DCM Block.

To design a clock divider circuit and one of the DCM output is given as an input to the clock divider block. The clock divider block performs both the counter and comparator operations. Counter block counts the number of times the event occurred in the clock pulse. In this method, output from the DCM block is taken as input and is divided

into number of stages. The number of stages will be counted by the counter which is present in the frequency divider. The counter value attain its maximum, the counter will be reset. And again starts count from 0 to N. Simulated output of the clock divider circuit is shown below.

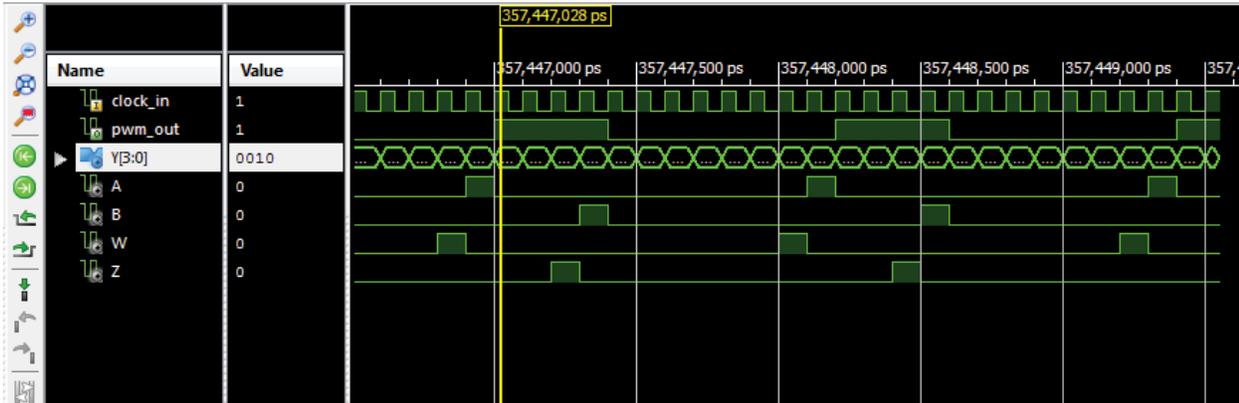


Fig.5 Pulse Width Modulated Output

TABLE I COMPARISON

POWER	EXISTING (nW)	PROPOSED (nW)
STATIC POWER	119.73	30.088
DYNAMIC POWER	55704.195	26536.225
TOTAL POWER	55823.925	26566.313

The table 1 shows the power comparison between existing and proposed system this shows the proposed method consumes less power than existing system.

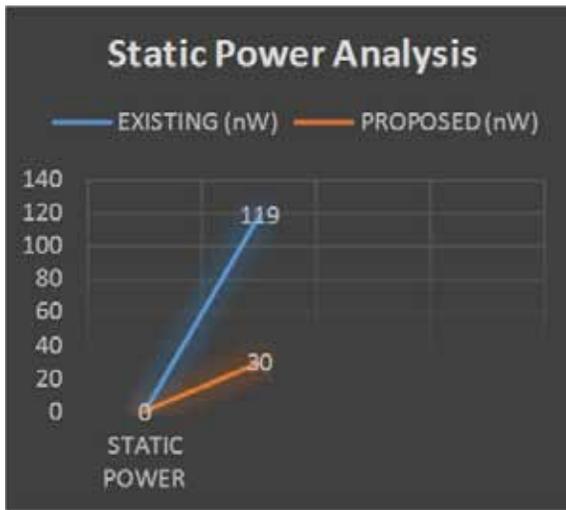


Fig.6 Static power analysis



Fig.7 Dynamic power analysis

V. CONCLUSION

Thus a new approach of Pulse Width modulation technique using Xilinx ISE is developed. The pulse width modulated signal is obtained and it is verified by Isim simulator. And the analysis are done by Cadence tool. Compared with Xilinx tool cadence tool is suited for analyzing Power, Area, and Timing.

REFERENCES

- [1] Denis Navarro, Oscar Lucía, Member, IEEE, Luis Angel Barragán, José Ignacio Artigas, Isidro Urriza, and Oscar Jiménez, Student Member, IEEE 'Synchronous FPGA-Based High-Resolution Implementation of Digital Pulse-Width Modulators' *IEEE transactions on power electronics*, vol. 27, no. 5, may 2012.
- [2] M. G. Batarseh, W. Al-hoor, L. Huang, C. Iannello, and I. Batarseh, 'Segmented Digital clock manager FPGA based digital pulse width modulator technique' in Proc. Power Electron. Spec. Conf., 2008, pp. 3036–3042.
- [3] A. de Castro and E. Todorovich, 'High resolution FPGA DPWM based on variable clock phase shifting,' *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1115–1119, May 2010.
- [4] A. de Castro and E. Todorovich, 'DPWM based on FPGA clock phase shifting with time resolution under 100 ps,' in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3054–3059.
- [5] S. C. Huerta, A. de Castro, O. Garcia, and J. A. Cobos, 'FPGA-based digital pulse-width modulator with time resolution under 2 ns,' *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 3135–3141, Nov. 2008.
- [6] M. Scharrer, M. Halton, T. Scanlan, and K. Rinne, 'FPGA-based multiphase digital pulse width modulator with dual-edge modulation,' in Proc. *IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1075–1080.
- [7] A. Syed, E. Ahmed, D. Maksimovic, and E. Alarcon, 'Digital pulse width modulator architectures,' in Proc. IEEE Power Electron. Spec. Conf., Jun. 2004, vol. 6, pp. 4689–4695.