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Adder with Efficient Speed and Area by Using Quantum-Dot Cellular Automata Technology

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Abstract **- The lessening in transistor estimate by following field's law made chip unpredictability with more computational capacity. The present size of the transistor needs to decrease more, which prompts nanotechnology. The quantum-dot cell automata come extremely close to nanotechnology presents one of the conceivable arrangements in defeat this physical breaking point, even though the designs with QCA technology are not a fundamental basic. In this brief by considering quantum-dot cell automata (QCA) innovation idea a greater part door based adder is outlined. The effectiveness in territory and speed by larger part entryway idea based adders are executed and contrasted with beforehand technique plans by utilizing verilog coding mimicked in Xilinx. The proposed one-piece QCA viper depends on another calculation that requires just three larger part entryways and two inverters for the QCA expansion. Novel 128-bit adders designed in QCA become accomplished.**
Keywords: **QCA, Nanotechnology, Majority gates (MG), adder, Verilog HDL**

I. INTRODUCTION

The largest part computer scientists and engineers nowadays are attentive regarding the reduction of transistor sizes, for it's been a hysterically development in vision with the intention of the beginning of vacuum tubes, and the purpose of swift enhancement of computing technologies. At the moment, we use CMOS (Complementary Metal Oxide Semiconductor) production to create our transistors. The blessings of CMOS making above diverse technology is that they encompass get rejection of stagnant electricity dissipation, frequent intellect ranges are extremely restored, integration degrees are high, and rising drive and fall transition times are of the same order. In the past, we were using micron technology. In 2001, we commenced the use of .25µm CMOS generation which is avowed to be deep sub-micron (DSM) generation. Other DSM technology encompasses the .180µm and the .130µm technology. Next we have nanotechnologies at transistor sizes of 90nm (.090µm), 65nm (.065µm), and 45nm (.045µm) [1]. Digital pc arithmetic is a fixation of ordinary intelligence design with the purpose of mounting suitable algorithms that allows you to collect an inexperienced utilization of the hardware [2-4].Boolean equations can easily performed, which are mathematical equations. Power delay areas are three parameters are the major criteria of any design.

Binary parallel adder (RCA), Look ahead carry adder (CLA), and dependent comprehensive adders were developed [5]. The addition operation for two binary numbers for n bits can be achieved by RCA or binary parallel adder. The designing of such a adder can be achieved by cascading n full adders. Through cascading the output carry of one full adder is connected as an input to another full adder and sum are collected. The carry propagating makes a delay in ripple carry adder. This delay effects in reducing speed of adder. Since many arithmetic functions like multipliers, subtractions etc depend on adders. So down the lane it can be understood the efficiency of arithmetic designs improves in terms of speed if delay rescues. Finally justifies the carry propagation time reduction makes impact in speed efficiency. To come across carry propagation delay problem different approaches are defined. One of the widely used approach is carry look-ahead adder, solves this problem by taking input signal and producing carry outputs [6].

In this brief, using QCA technology an innovative attention way of designing low area and less speed adders is presented. The entire QCA technology is based on majority gates. Using the majority gates techniques CLA and binary parallel adder (RCA) are implemented and evaluated. This paper is organized with section II followed by data of QCA, and data regarding majority gates. Section III follows basic architectures of adders which we considered in these papers (RCA and CLA). Section IV considered proposed methods. Section V goes with results.

II. QCA TECHNOLOGY

The fundamental limit of CMOS technology is impacting the engineers to move for nano technology in new era. One of the nanotechnologies QCA nano technologies is deals here. This technology is completely transistor less beyond CMOS technology. The complete state of art survey on QCA is presented in this paper. This paper addresses the QCA background. The work of QCA depends on flow or moment of electrons and operations are done by the arrangement of electrons in a square cell with 20 nanometers. These quadratic cells are technically termed as QCA cells. In these square cells four dots are presented called as potential wells. In this potential wells electrons will get locked [8]. This potential wells with electrons gives the values either logic 1 or logic 0.The connection between these potential wells is attained by tunnel junctions. These junctions give a path for electrons to move that to in

controlled path, by a clock signal. The moment of electrons to far distance without any outside noise is practiced here by the columbic force that interacts between them. As the diagonal is the more distance path between the electrons, they get resided in diagonal potential wells.

Fig. 1 QCA cell representation

The above shown figures reflect the diagonals, electrons in potential wells. The logic 1 and logic 0 can be judged by the above representations of cells, i.e. each cell can be in two states as discussed above. The state '0' and the state '1'.Arrays of collaborating QCA cells have been established to prepare to do all the rationale capacities required for all wide-ranging advanced outline. QCA dots are obstructed by potential energy which is controlled by QCA clocking. Exchanging in QCA is proficient because we can interchange the electrons in adjacent cells by potential energy. By this association signs of the QCA can be recognized [8]. The topology of the QCA design decides the assistance of the cells and thus the usefulness of the general circuit. The power drop of QCA is low since just two electrons are moving. The majority of the power required by QCA circuits will be utilized by the timing plan [7]-[8].

A. QCA Clocking

By controlling potential boundaries between the quantum dots timing can be attained for QCA. Challenge that we face here is clocking as it plays tricky role. The data path for data propagation is achieved by this Clocking, through QCA circuits. Clock cycles are in contrast to CMOS, here in one clock cycle totally four clock cycles are studied with delay of 0.25 each. These QCA clocking is having four phases switch, hold, release and relax. In switch phase the unpolarised cell get polarized either for Binary 0 or Binary 1. In hold phase whatever the polarized value is attained is get hold to pass that data to other cell or for the other input. The release phase help the cell to get unpolarized, and get relaxed in relax phase [9].

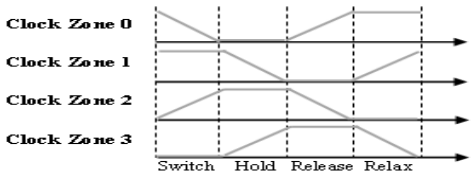

Fig. 2 QCA clocking zones

The means of controlling is attained by attaching cells adjacently. The below figure depicts different clocking zones clock 0,clock 1,clock 2,clock 3 by gray shadings.

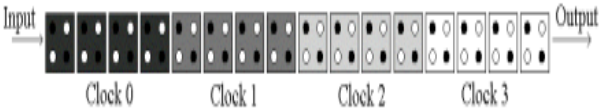

Fig. 3 clocking layout

B. QCA Logic

For efficient way of transferring information or data through QCA, to get wire layout succeeding clocking zones are connected. This guides QCA data to transmit. QCA wire is formed by an array of QCA cells shown in Fig, wire act as an intermediate for passing data.

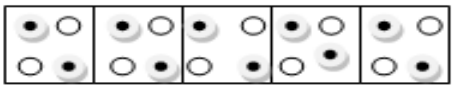

Fig. 4 QCA wire

There is a rough upper limit for the size of one clock zone. In QCA wires with almost no other QCA cells near the wire, i.e. with no Coulomb force noise from the surrounding, clock zones can be large. The clock zones path should be designed in smaller path. The size of the clock zone doesn't depend on noise there no, mandatory rule for that. Through QCA layouts a computation in QCA is proficient, which display the preferred communication of states. The figures in 5 present the layout for majority gate and inverter in QCA.

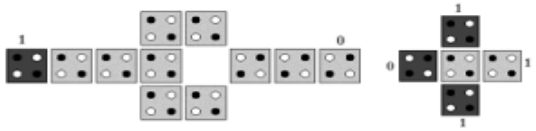

Fig. 5 Inverter and majority gate layouts

In QCA designing NOT gate is a bit crucial zone, so arranging cells properly to get NOT functionality is important to avoid miss communications of electrons. The input clock zone should get end at the starting stage of fork. It should be maintained that input should be maintained in one clock zone subsequently output should be checked in next clock zone. Majority gate is designed with the cells which are in same clock zone. Instead of adjacent clock zones different clock zone may lead to wrong results. The center cell and the three inputs plus the output cell have to be in the same clock zone. The fundamental or basic of QCA technology is majority gates. Through the input polarization output polarization is attained. AB+BC+CA are the majority gate equation, with respect to inputs A, B, C. In this equation of majority gate by keeping constant values to 0 or 1 for any of the inputs AND and OR logic can be performed [9]-[10].

III. REGULAR METHOD

A. Basic Full Adder Block

The logical gates such as AND gate, OR gate, NAND gate etc. are used to implement many arithmetic technologies, among all this operations multiplications, subtractions, divisions addition is the common part. Changing the functions of addition all the reaming arithmetic operations can be performed.

Two types of basic adders are half adder, which adds two inputs and full adder which adds three inputs. Full adder is designed with totally three inputs input A,B along with

carry input cin and produces outputs carry and sum. The sum output of full adder is performed by xor operations of inputs A, B, cin as A xor B xor cin, and carry output as AB+BC+CA [11]. The truth table and block diagram are shown below.

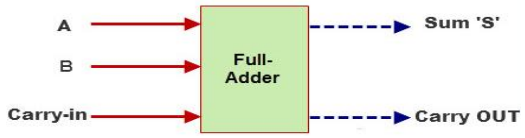

Fig. 6 Full adder block diagram

TABLE I FULL ADDER TRUTH TABLE

Inputs		Output		
A	B	C-IN	C-OUT	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

B. Ripple Carry Adder or Binary Parallel Adder

The 1 bit range three inputs can be added using full adder as discussed above. If n bits are too added then we can go for the design of RCA. Ripple carry adder is designed by cascading n number of full adders and giving one constant input cin.

The cascaded stages are fed with the cin inputs as the previous carry output of previous full adder. As each bit rippling to next stage this type of adder is named as a ripple carry adder or binary parallel adder. This adder can be designed by taking n full adders for n bits and also by taking n-1 full adders and 1 half adder also.

The n bit in ripple carry adder are added by designing cascaded connections of full adders as shown in Fig.7.Out of n bit input range, the i th bit position values produce i th bit summation and carry out c_i for next stage input, to the next adder stage. This is called a Ripple Carry Adder (RCA), the carry get ripples form LSB to MSB [11].Since carry out is rippling for n stages total delay it faces is 2n. The path taken for output from input to output is critical path, which is an initial input to final sum output.

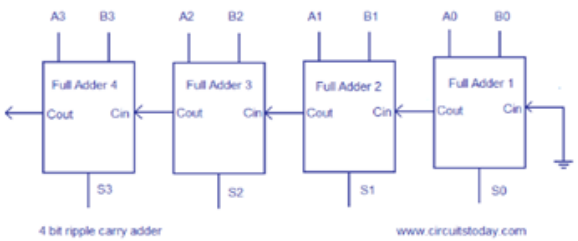

Fig.7 4 Bit RCA architecture

C. Carry Look Ahead Adder

As of having critical path from initial value to final sum output, this delay is more in ripple carry adder. 2N+1 is the critical path delay of RCA. This delay tends to be reducing in speed and complex in implementing. So the alternating attracting design is carry look ahead adder [12]. The delay problem can be reduced here and speed efficiency can be gained. The carry look ahead design can be obtained by a transformation of the ripple carry design into a design in which the carry logic over fixed groups of bits of the adder is reduced to two-level logic.

Carry propagation time is a deterrent characteristic on the speed by means of which two numbers are added in parallel. In vision of the aspect that all other arithmetic operations are implemented by consecutive additions, the time consumed through the addition procedure is very significant. An understandable explanation for dropping the carry propagation delay time is to make use of faster gates with reduces delay. But physical circuits have a bound to their capacity. There are numerous techniques for dropping the carry propagation time in parallel adder. The mainly extensively used technique employs the principle of look-ahead carry. The functioning of carry look ahead adder is discussed here. The carry look ahead adder using the concept of propagating and generating the carry bit. It calculates one or more carry bits before the sum, which reduces the wait time for complex calculations.

Let us imagine that A_i and B_i are the inputs of an adder i.e. full adder stage, and C_i is its carry input. The look ahead carry output is then expressed by (1), and the sum output is expressed by (2).

$$C_{i+1} = G_i + P_i + C_i \quad (1)$$

$$Sum_i = P_i + C_i \quad (2)$$

The binary full adder is a input arithmetic unit that include two information bits comprehensive of any approaching convey information and produces the sum and carry (over flow) yield. In (1) and (2), Gi and Pi speak to create and engender signals, where Gi = AiBi and Pi = Ai⊕Bi. Item suggests sensible conjunction, and entirety infers intelligent disjunction in the conditions. The image ⊕ determines intelligent selectiveness (i.e. sensible XOR). Notice that create and spread capacities are fundamentally unrelated – consequently the convey is either produced from a viper arrange or the convey just engenders from the contribution to yield. Conditions (1) and (2) are innately in disjoint aggregate of items (DSOP) or total of disjoint items shape. In such a shape, any two item terms constituting the Boolean articulation would be commonly orthogonal i.e. the coherent conjunction of any match astute mix of the item terms would compare to invalid (i.e. twofold 0).

Loosening up the recursion implicit in (1), the express look ahead carry yields comparing to a 4-bit convey look forward generator are indicated by (3) to (6), where C0 speaks to the communicate involvement to the 4-bit carry look forward

generator, and C1, C2, C3 and C4 speak to the relating look forward convey yields produced. Notice that in a non-specific m-bit CCLA, a sum of m look forward convey yields are delivered. Conditions (3), (4), (5) and (6) demonstrate what the look like ahead convey are reliant just upon the approach. Contribution to the convey look forward generator. Conditions (3), (4), (5) and (6) are naturally in DSOP shape.

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0 \quad (3)$$

$$C_3 = G_3 + P_3G_1 + P_2P_1G_0 + P_2P_1P_0C_0 \quad (4)$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_0 \quad (5)$$

$$C_1 = G_0 + P_0C_0 \quad (6)$$

The below fig. 8 reflects the n bit conventional carry look ahead adder. The three steps the carry look ahead adder permits are

1. To give propagate generate signals of input bits we have to give logic for propagation and generation.
2. This n bit carry look ahead adder considering generated and propagated signals along with input carry C0 propagates sum and generates carry as output and also as an input for next stage.
3. The sum logic, which combines the respective propagate and carry signals of the n-bit CCLA according to (2) and sum outputs of adder are processed.

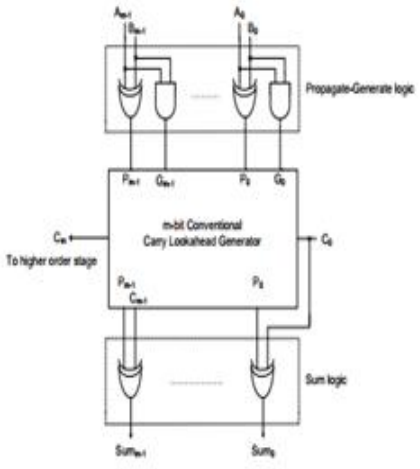

Fig. 8 Structural representations of carry look ahead adder

IV. PROPOSED METHOD

First full adder layout is proposed by the University of Notre Dame. Since QCA is based on majority gate logic based design, for the design of full adder same majority logic and gate is used. Reduction of sum of product logic to majority will almost always lead to smaller layouts, which is the most important advantage in QCA [13]-[14].

A. Novel RCA Adder

Ripple carry adder or binary parallel adder layout in QCA can be easily attained, which allows faster designs means efficiency in speed. Binary parallel adder (RCA) gives more delay, as each stage of full adder is to stay for carry bit, as it should be given for next stage. Majority gate based designs for carry look ahead adder and ripple carry adder is designed and are shown below

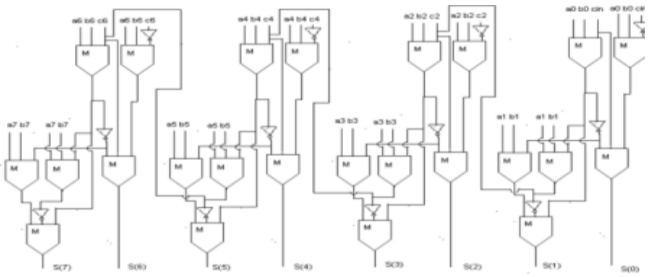

Fig. 9 Ripple Carry Adder Using Majority Gate

B. Novel CLA Adder

QCA layouts are implemented by QCA cells, crossovers and bridges are also implemented with QCA cells. The primary logic gates are developed by using majority gates by giving constant values as 0 out of one input in three inputs a, b, and c, we can design AND gate and making constant as 1 one can perform OR operation.

$$M(a,b,c) = a \cdot b + a \cdot c + b \cdot c. \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

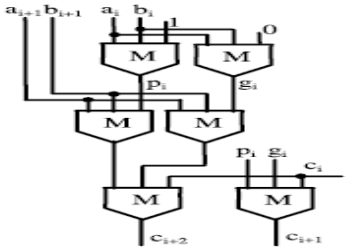

Fig. 10 New 2 bit design with majority gates module

Sum propagate signal and carry generate signal can be attained by pi = ai + bi and gi = ai.bi, this operation is processed for each stage and finally sum of all stages are collected. Such a planned n-bit CLA has a computational way gathered of 7+4× (log4 n) fell MGs and single not entryway. This can be effectively confirmed by looking atgiven, the spread and create signals (for which just a single MG is required), to process gathered proliferate and assembled produce signals, four fell MGs are presented in the computational way. Moreover, to develop the communication signals, one level of the CLA rationale is crucial for each aspect of four in the operands length. This implies, to process n number of bit addends, log4 n levels of CLA rationale is required, each adding to the computational way with four fell MGs. At long last, the calculation of total bits presents two further cell MGs and one inverter.

V. RESULTS

The proposed majority gate of QCA technology based adder (RCA and CLA) is implemented. Xilinx ISE simulator is used for implementing the designs and outputs are verified by simulating the designs.

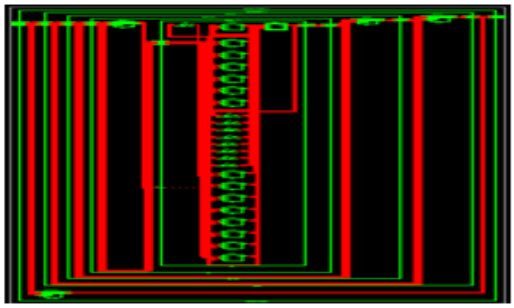

Fig. 11 RTL schematic of RCA

The above fig.11 shows the RTL schematic of ripple carry adder, which contains internal blocks and connections of the design.

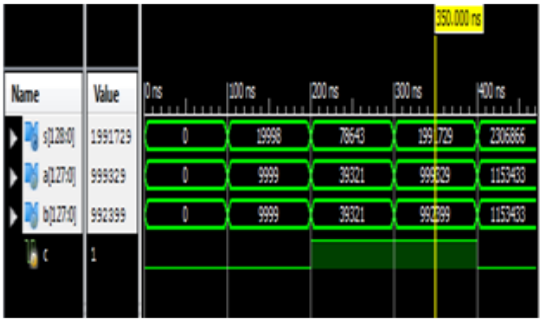

Fig. 12 RCA output waveforms

The output waveforms of RCA are shown in above figure

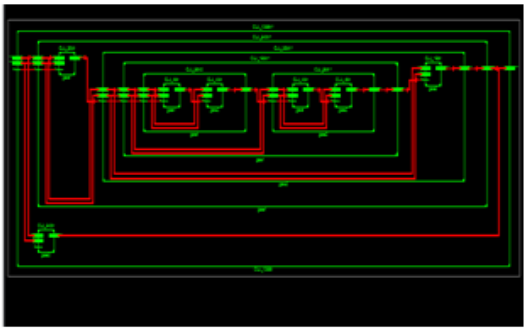

Fig. 13 RTL schematic of CLA

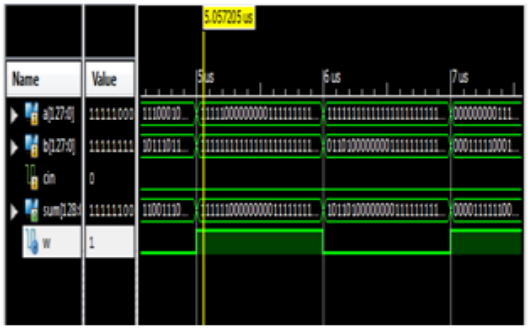

Fig. 14 CLA output waveforms

Similar to above RCA RTL and output waveforms CLA RTL block figure and output wave forms are shown in above figures. The comparison table here presents the slice LUTs, bounded input output bonds and delay parameters. By synthesizing the adder codes based on majority logic in Xilinx we attain the parametric values of area and delay. The results show our novel designs are efficient in terms of speed an area.

TABLE II COMPARISON TABLE

128bit Type/Parameter	Slice Luts	Bonded IOBs	Delay (ns)
Conventional RCA	193	386	30.319
Novel RCA	208	386	37.117
Conventional CLA	192	386	29.974
Novel CLA	193	386	26.208

VI. CONCLUSION

Quantum dot cellular Automata is one of the nanotechnology suits for designing digital circuits based on majority gate based logic, among all digital circuits adders plays a major role. Majority gate is a powerful block of QCA. Area and delay are the concern parameters of VLSI, These parameter variation among the majority gate based novel RCA adder and CLA adder are presented and get compared with regular method design of conventional RCA and CLA adders. The carry look ahead adder with majority gate design outperform in delay with passable area over regular way design. The parameter comparison is done here in this paper by considering results in Xilinx ISE simulator.

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