Capacitive Fringing Field Sensor Design for Moisture Measurement

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***Abstract* – The fringing field capacitive sensor is described for moisture measurement like soil, food application. Interdigitated electrode capacitive sensor has been utilized in numerous applications at low frequency. A sensor performance was evaluated by monitoring the output capacitance variation with and without moisture content. The variation in capacitance is directly measured by using interface circuit. Switched capacitor dual slope capacitor to digital converter has been utilized as an interface circuit. The interface circuit has been designed and simulated with variable capacitance by sensor performance. Printed circuit board technology is particularly advantageous for realizing this type of sensor by fabricating the interdigitated electrode structures in the patterned Cu foil instead of realizing these type of sensors in various technologies.**

Keywords: **Fringing field sensor, Interdigitated electrode, Moisture measurement, DSCDC**

I. Introduction

Capacitor structures can be utilized as sensors for numerous applications. The sensors can measure many physical variables (measurand) like position, accelerometer, moisture, angular speed and liquid level to detect the environmental changes. The changes in the capacitance of the sensor was monitored for any measurand that affects the electrode separation distance, the electrode overlapping area, or the relative permittivity of the dielectric in the vicinity of the electrodes. A useful sensor can be realized by additionally interacting with the fringing fields for any measurand (i.e moisture), thereby reconfiguring the electric displacement field (D) mapping and changing the measurable capacitance due to the fringing field. Fringing field capacitor sensors have the advantage of projecting the fringing field into the object or material without altering the electrode configuration. Interdigitated electrode structures are particularly suitable for this sensing technique since they can be designed to maximize the capacitance due to fringing. Capacitive sensor uses the method of measuring changes near the sensor's surface which is considered as the distinct advantage when compared to other techniques explained in non capacitive sensor [1-5]. The capacitive sensor measurements do not possess potential health risks of radiation-based methods. Fabricating and operating low-frequency capacitive sensors are simple relatively compared to RF-based techniques. Switched capacitor dual slope capacitance to digital converter [6] is used for sensing capacitance-type sensor in several areas as they provide better sensitivity and linearity of any measurand.

Fig. 1 Block diagram of capacitive sensor

Typical ADC possesses an analog part and a digital part which is required to interface a capacitive sensor. An analog part of an ADC itself is designed to accept the elements of a sensor and the ADC logic is appropriately modified to provide a digital output directly proportional to the parameter being sensed. An analog signal-conditioning circuit that converts the variations in the sensor capacitances to a proportional analog voltage or current is required in an analog to digital converter. Such a scheme does not require a separate analog-signal-conditioning unit. A direct conversion method provides an output proportional to the ratio of two capacitances which is suitable for differential capacitive sensors has been proposed in [7]. Hence, direct conversion method can observe a small range of variations in the capacitances of the sensor. A novel switched-capacitor dual-slope technique that converts the variations in the capacitances C1 and C2 of a differential capacitive sensor directly into a proportional digital value based on a ratiometric approach was presented [8]. The proposed dual-slope CDC (DSCDC) offers an advantages of negligible sensitivity toward various error sources, such as stray capacitances, switch leakage currents, and op-amp

offset voltage, high speed in comparison with the delta sigma interface circuit[9] and charge amplifier circuit[10]. Moreover, this method requires only a single dc reference voltage and hence avoids errors arising out of mismatched dc reference voltages (offset voltage) of opposite polarity, which is a major source of error in the triple-slope CDC scheme.

II. Interdigited Electrode Structure

Consider a structure where n plates, referred to as electrode teeth, of area, a, are stacked in parallel, a fixed separation distance, d, apart, in a dielectric material of relative permittivity, εr, as illustrated in the top-view drawing in Fig. 2. Every other electrode tooth is electrically connected together through a common electrode arm. This electrode configuration is referred to as two interdigitated electrodes. In the drawing, "A" and "B" are the electrical contacts to the two interdigitated electrodes.

If the magnitude of the overlapping tooth area is much greater than the electrode separation distance, most of the capacitance between opposing teeth is due to electric flux directly between the electrode overlapping areas and is not due to fringing effects. However, since the perimeter around the teeth is much greater than the perimeter around two parallel plate electrodes of the same total overlapping area with the same electrode separation distance, the fringing effects will be considerably greater in the interdigitated electrode case.

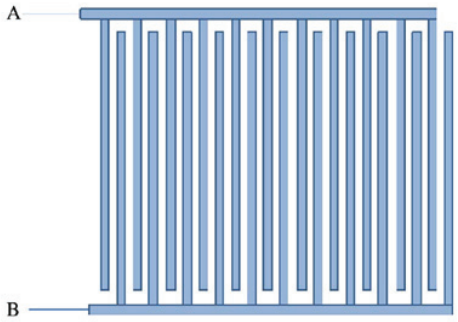

Fig. 2 Top view of interdigitated electrodes

For n interdigitated electrode teeth, the equation for the capacitance can be approximated as

$$C = \varepsilon r\ \varepsilon o\ a\ \gamma / d \tag{1}$$

where εo is the permittivity of free space, 8.854 pF/m, and γ is the fringing scale factor which is equal to or greater than one. Equation (1) does not account for the case where multiple materials possessing different relative permittivity values are in contact with the electrodes. It also assumes that the capacitance between the ends of the teeth and the arms to which the opposite electrode teeth are physically attached is negligible. If the height of the teeth is on the same order as the separation distance, much of the capacitance will be due to the fringing fields outside of the space directly between the interdigitated teeth and γ will be significantly greater than one.

III. Finite Element Simulation

A finite element is used as the basis for the simulations that solve the Maxwell equation ($\nabla D = \rho_f$) subjected to the appropriate electromagnetic boundary condition. The classic electrostatic boundary conditions are assumed as the tangential component of the electric field across dielectric interface is continuous ($E_{t1}=E_{t2}$) and the normal component of the electric flux density is continuous at the surface ($D_{n1}=D_{n2}$) from the Maxwell equation of

$$\nabla . D = \rho_f \tag{2}$$

$$D = \epsilon E \tag{3}$$

$$E = -\nabla \varphi \tag{4}$$

where ρ_f is free charge density, D is electric flux density, E is the electric field intensity and φ is electric potential.

A two dimensional finite element analysis (FEA) simulation was conducted to examine the degree of field fringing that occurs in the vicinity of the electrode-surface region. The finite element simulation was performed in 3D or 2D depending on the application specific. The cross-sectional area of the sensor arm is invariant with length, thereby reducing the problem to a 2D solution of the Laplace equation.

$$\nabla^2 V = 0 \tag{5}$$

where V is the electric potential. Galerkin's method was employed for the numerical solution to the hyperbolic problem using standard six-node triangles. In the solution, the algebraic equations were solved using Gaussian elimination. All conducting surfaces were approximated as perfect electric conductors, and the continuity of the normal component of the electric flux density (D=εE) maintained at the dielectric-air interface

$$\Sigma_1 \frac{\partial V}{\partial n} = \Sigma_2 \frac{\partial V}{\partial n} \tag{6}$$

where *n* is the unit vector perpendicular to the dielectric–air interface.

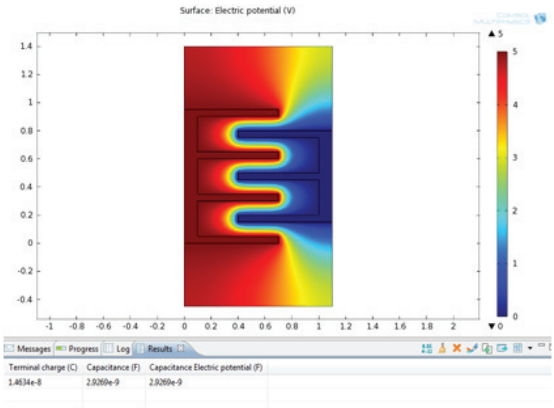

Fig. 3 Finite element simulation of IDE sensor

Here interdigitated electrode structure is used as sensor which is developed using finite element simulation. In FEM, one sensor arm is given as the required voltage and other sensor arm is to be grounded. This differential voltage produces the capacitance value by changing the permittivity. The capacitance value is calibrated between air and water with same material. Similarly, since water has an εr value approximately 80 times greater than that of air, the water content of many common materials into which the sensor is fully submerged may be estimated.

IV. Interface Circuit

A. Push-Pull Capacitive Sensor

A differential capacitive sensor has two sensing capacitances *CS* and *CR* whose values change in proportion to the parameter being sensed, and the changes in *CS* and *CR* are normally equal and opposite. Since the value of one of the capacitances increases and that of the second capacitance kept constant being sensed, differential capacitive sensors are also popularly known as push–pull-type capacitive sensors.

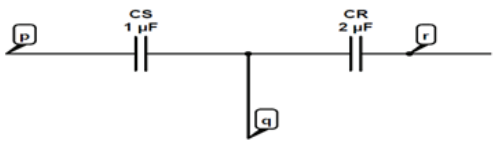

Fig. 4 Differential capacitive sensor

A simplified electrical equivalent circuit of a typical differential capacitive sensor is shown in Fig. 4. If the parameter being sensed alters the area between the plates of the sensor, then such a capacitive sensor will possess a linear input–output relationship, as given by the following

$$C_S = C_0 (1 \pm kx) \quad (7)$$

Here, k is the transformation constant of the sensor, and $C0$ is the nominal value of $C1$ and $C2$, when x, which is the physical quantity being sensed, is zero. The switched capacitor dual slope capacitance to digital converter is based on differential capacitive sensor.

V. Switched Capacitor DSCDC

The functional block diagram of the proposed DSCDC is shown in Fig. 4. As in any dual-slope technique, the DSCDC is made of an switch, integrator and a comparator. As indicated in Fig. 4, the sensor capacitance CS and CR in combination with three single-pole double-throw (SPDT) switches SW1, SW2, and SW3, opamp and the feedback capacitor *Cf* form a switched-capacitor integrator. The status of the output of the integrator is sensed by the comparator.

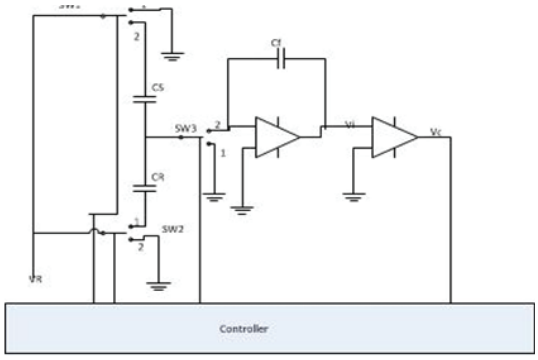

Fig. 5 Block diagram of DSCDC

VI. Conversion Cycle

A typical conversion cycle consists of two time periods, which is T1and T2. While the period T1 is a preset value, *T*2 is measured. During T1, when the clock is high (TC/2), switch SW2 is set at position 2, and switches SW1 and SW3 are set to position 1. When the clock turns low, switch SW2 is changed to position 1, and SW1 and SW3 are set to position 2. Thus, whenever the clock is high, CS will charge to VR, and CR will get discharged to ground. As soon as the clock goes low, the charge in CS will be transferred to CF , and at the same time, the charging current of CR is also sent into CF. Hence, the differential charge between VRCS and VRCR, i.e., VR (CS − CR), will get transferred to CF for every clock cycle. If CS > CR, then Vi ramps in the positive direction in steps of value VR (CS − CR)/CF for every clock period TC, as indicated by the solid line in Fig. 6. On the other hand, if CR > CS, then voi will ramp in the negative direction in steps

of value VR (CR-CS) /CF for every clock, as indicated by the dotted line in Fig. 6. If CS = CR, then the differential charge transferred to CF for every clock is zero; hence, at the end of T1 (= N1TC, with N1 being a preset integer), the output of integrator Vi will remain zero.

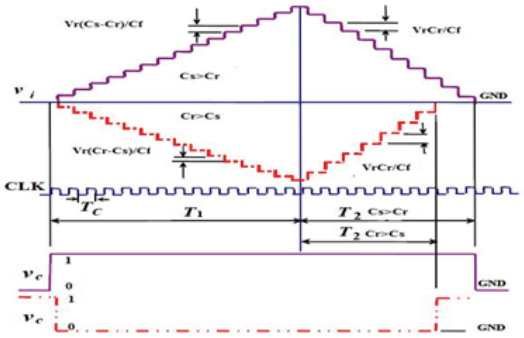

Fig. 6 Integrator output and comparator output

The second integration period T2 commences as soon as the period T1 is completed. If Vc is high at the end. of T1 (i.e., CS > CR), then switches SW1 and SW3 to position 2 and SW2 to position 1 whenever the clock is high and whenever clock is low, SW1 to position 2, SW2 to 2 & SW3 to position 1 is connected. Thus, when the clock is high, *C*R will get charged to VR, and their charging current will discharge CF by VRCR/CF. When the clock goes low, both sensor capacitances and reference capacitance are discharged to ground. This process is repeated for every clock cycle.

Fig .7 Flowcharts for conversion cycle

Hence, the output of the integrator gradually decreases in steps of VR (CR)/CF and reaches zero. On the other hand, if Vc is low at the end of T1 (i.e.,CR > CS), then switches SW2 and SW3 switched to position 1 and SW1 switched to position 2 whenever the clock is high and changes the switches SW2 and SW3 to position 2 and keep switch SW1 in position 2 whenever the clock turns low. Thus, when the clock is high, both CR will get charged to *VR*. In addition, when the clock goes low, their net charge VRCR is transferred to CF, discharging it. Under this condition, Vi increases in steps of VR (CR)/CF and reaches zero, as indicated by the dotted line in Fig. 6. A flowchart showing the sequence of operations and switch positions during the periods T1 and T2, depending on the comparator output voltage Vc, is shown in Fig. 7.

At the end of period T2, the net charge in CF is zero. As per the equation $C_S = C_0 (1 \pm kx)$, set CR=C0, Then T2 will become,

$$\frac{T_2}{T_1} = \frac{C_0(1 \pm kx) - C_0}{C_0} \tag{8}$$

which is equal to ±kx. We know $N_2 = \frac{T_2}{T_c}$ and $N_1 = \frac{T_1}{T_c}$ then

$$\frac{N_2}{N_1} = \frac{T_2}{T_1} = \pm kx \tag{9}$$

N1 is the preset value from T1 and we can calculate the digital value from known value of N1, T1 and integration value.The following graph shows the response of dual slope converter. Since *N*1 is a preset value and *k* is the sensor's transformation constant, the digital value *N*2 directly represents the quantity *x* being sensed by the sensor. Thus, the technique presented here implements a linear direct CDC applicable for not only differential capacitive sensors possessing linear characteristics but also sensors possessing inverse characteristics without any change.

VII. Simulation Result

A. Capacitance Measurement

The sensor capacitance is measured by using COMSOL tool. COMSOL tool is mainly based on Maxwell equation. Finite element method is used to determine the capacitance. COMSOL is one of the tool using finite element method. It gives the output either in 2D or 3D. COMSOL Multiphysics is an interactive engineering and physics tool that performs equation based modelling in a visual interface. This software allows the modelling and simulation of any physical

phenomena in a way that's easy to implement. It comes preinstalled with different model libraries that can be readily used. Some of the libraries include modules such as Chemical Engineering Modules, MEMS Modules, RF Modules and Structural Mechanics Module.

Electrostatics part of MEMS module is used in 3D. 3D electrostatics problem by first creating a 2D geometry using the array tools and then extrude it to a 3D geometry, perform Mesh analysis and compute the capacitance using the Electrostatics application mode's port boundary condition. The simulation result and its corresponding capacitance value using COMSOL software is shown below in figure 8 and Table I.

TABLE I CAPACITANCE VALUE FOR DIFFERENT PERMITTIVITY VALUE

Permittivity(ε)	Capacitance (F)	Charge(Q)
1 (Air)	9.9578e-14	4.9789e-13
2	1.9916e-13	9.9578e-13
3	2.9873e-13	1.4937e-12
4	3.9831e-13	1.9916e-12
5	4.9789e-13	2.4895e-12
6	5.9747e-13	2.9873e-12
80(Water)	7.9663e-12	3.9831e-11

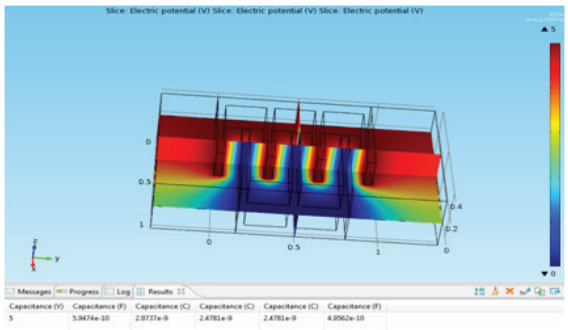

Fig. 8 Charge variation using COMSOL

VIII. INTERFACE CIRCUIT

The capacitance mentioned in the above table is measured digitally. It can be performed by using analog to digital converter. Here dual slope type of ADC is used. Digital representation corresponds to difference in sensor capacitance and reference capacitance. The clock signal and square wave pulse is used to control the switches. It is simulated using SPICE software and the response is obtained. The modified output is shown in Figure 9.

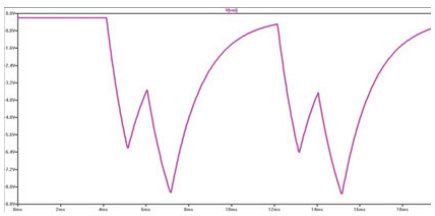

Fig. 9 Output from SPICE

VI. CONCLUSION

Capacitive sensors have been utilized for the detection or measurement of water content. Most of these sensors utilize some type of interdigitated electrode structure. Low-cost capacitive fringing field sensor technology based on standard PCB technology has to be developed. Capacitance is found by using this technology is lesser in comparison to the other technology. At low cost and low frequency, the proposed sensor has been developed. Conversion time is good as a typical dual slope ADC and the proposed technique has high accuracy. The sensor capacitances become an integral part of a dual-slope converter, and the converter logic has been chosen, such that it provides a digital output directly proportional to the parameter being sensed by the sensor.

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